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FRONT-END ASIC FOR HIGH RESOLUTION X-RAY SPECTROMETERS*

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Front-end ASIC for High Resolution X-Ray Spectrometers

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Abstract -- **We present an application specific integrated circuit (ASIC) for high-resolution x-ray spectrometers. The ASIC is designed to read out signals from a pixelated silicon drift detector (SDD). Each hexagonal pixel has an area of 15 mm² and an anode capacitance of less than 100 fF. There is no integrated Field Effect transistor (FET) in the pixel, rather, the readout is done by wire-bonding the anodes to the inputs of the ASIC. The ASIC provides 14 channels of low-noise charge amplification, high-order shaping with baseline stabilization, and peak detection with analog memory. The readout is sparse and based on low voltage differential signaling. An interposer provides all the interconnections required to bias and operate the system. The channel dissipates 1.6 mW. The complete 14-pixel unit covers an area of 210 mm², dissipates 12 mW cm^{-2}, and can be tiled to cover an arbitrarily large detection area. We measured a preliminary resolution of 172 eV at -35 C on the 6 keV peak of a ^{55}Fe source.**

I. Introduction

The work discussed here is part of a joint effort between the NASA Marshall Space Flight Center (MSFC) and Brookhaven National Laboratory (BNL) to develop a prototype high-resolution x-ray spectrometer (XRS) able to measure the abundances of light elements fluoresced by ambient radiation. There are two possible uses being explored for this effort. The first application involves mapping the lunar surface from a low-altitude orbiter [1,2]. The second application is mapping the elemental composition of the surface of Europa [2,3].

A lunar mission requires a detector area of 500 cm^2, and able to offer an energy resolution better than 170 eV at 2 keV for rates up to few thousand counts s^{-1} cm^{-2} in a power budget of 20 mW cm^{-2}. The Europa application requires a detector area of 10 cm^2, and able to offer an energy resolution better than 130 eV at 280 eV for rates up to one million of counts s^{-1} cm^{-2} in a power budget of 80 mW cm^{-2}. Detector cooling, not included in the power budget, can be provided in both cases for operations down to -35 C.

The stringent requirements on the detector's area, resolution, rate, and power suggest either using standard silicon diodes with high pixelation (a pixel area of few hundred μm^2) and bump-bonded front-end electronics, or employing silicon drift detectors (SDDs) [4], [5] with moderate pixelation (a pixel area of few tens of mm^2) and wire-bonded front-end electronics. As discussed in the next Section, the latter solution appears more attractive in terms of resolution, interconnects, and charge sharing.

Other research groups reported promising results in terms of rate and resolution with pixelated SDDs with the input transistor (e.g. junction field effect transistor, JFET) integrated with each pixel [8-13]. However, intergrating the FET imposes an additional technological challenge, might impose a lower limit in the power dissipation (some mW in the JFET itself), and requires somewhat higher complexity in the front-end electronics and interconnects to achieve the required stability, especially at high count rates [14-20].

We propose an XRS prototype based on a pixelated SDD sensor without an integrated FET. The anodes of the SDD array are directly wire-bonded to the inputs of the low-noise multichannel application specific integrated circuit (ASIC) as presented here.

In Section II we discuss the criteria for choosing the sensor, and in Section III we introduce the detector's architecture. Section IV illustrates the ASIC architecture along with some details of the circuit. Section V reports some preliminary experimental results.

II. Criteria for Selecting the Sensor

To be compatible with both the lunar and Europa applications the XRS must satisfy the following requirements: area 500 cm^2, resolution 130 eV at 280 eV, and rate 1 Mcps/cm^2, with a power budget of 20 mW/cm^2. An advantage for both cases is that the XRS can be operated at temperatures down to -35 C.

Assuming that a silicon sensor is chosen, the requirement of a 130 eV resolution at 280 eV translates into a minimum electronic resolution of 15 electrons rms, including the noise from the pixel leakage current and the charge amplifier's continuous reset. This is illustrated in Fig. 1 where the total FWHM is simulated as function of the x-ray energy, assuming an equivalent noise charge (ENC) of 15 electrons. Fig. 1 also reveals the relatively small contribution from statistic fluctuations at 280 eV (Fano = 0.11).

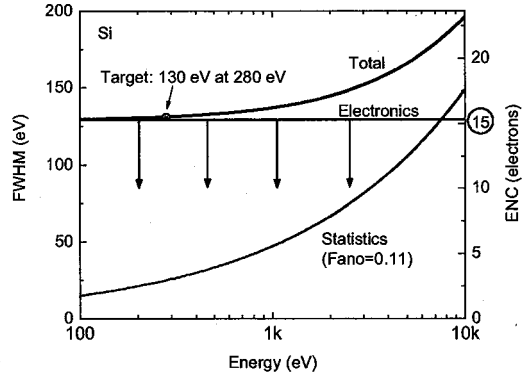

Fig. 1. Simulated FWHM as function of the x-ray energy assuming an ENC of 15 electrons rms. The contributions are also shown from the statistics with a typical Fano coefficient 0.11 and from the electronics, which must include the parallel noise from the leakage current and charge amplifier continuous reset.

Assuming a high-order shaper with peaking time equal to one-tenth of the inverse of the pixel rate ρ_{px}, the requirement of 10^4 counts s^{-1} mm^{-2} translates into a constraint on the maximum peaking time τ_p that depends on the area of the pixel A_{px} according to

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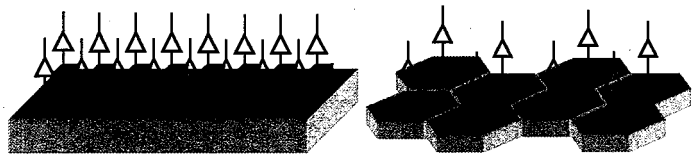
$$\tau_p \le \frac{0.1}{\rho_{px}} = \frac{0.1}{10^4 A_{px}} = \frac{10}{A_{px}} \left(\frac{\mu s\ mm^2}{mm^2} \right) \quad . \qquad (1)$$

For example, for a pixel of 10 mm^2 the peaking time should not exceed 1 μs.

We analyzed two solutions, the first based on standard Si pixels, as shown in Fig. 2(a), and the second based on SDD pixels (Fig. 2(b)).



(a) (b)

Fig. 2. Two possible solutions based on standard pixels (a) and SDD pixels (b).

We can now evaluate the achievable ENC as a function of the pixel area using the techniques discussed in [21]. We assume a typical leakage current of 1 nA/cm^2 at room temperature and an available power of 20 mW/cm^2, and we reserve 200 μW to each channel for signal processing (shaping, peak detection); the rest of the power is available for the input MOSFET branch of the charge amplifier. We assume operation at -35 C, and a capacitance of about 320 fF/mm^2 and 60 fF/mm, respectively, for the area and fringe of the standard pixel (these values were obtained from a field-solving based simulator, assuming a Si thickness of 300 μm), and of about 90 fF for the anode of the SDD pixel. Finally, we assume an interconnect capacitance of 100 fF, which encompasses the ASIC bond pad, and the bump-bond or wire-bond connection from the ASIC to the pixel.

In Fig. 3, the achievable ENC is plotted as function of the pixel area for the two cases in Fig. 2 along with the contributions from series- and parallel- noise. For this comparison, we assumed a CMOS 0.25 μm technology. The corresponding optimum peaking time is also shown. This comparison shows that the required resolution can be more easily achieved with SDD pixels, also offering a much broader selection of pixel areas. Other advantages are the charge sharing that decreases in a first approximation with the square root of the pixel area [6], [7], and the interconnect requirements, which due to the ≈ 650 μm^2 pixel area of standard pixels, would require either a low-loss interposer or bump bonding. The drawbacks of the SDD solution might be considered the higher complexity of the sensor and the additional supplies needed for the sensor on the pixelated side.

Consequently, we selected the SDD solution, with single pixel area of 16 mm^2 and an optimum peaking time of about 750 ns. We note that the optimum peaking time also satisfies the rate constraint (1). The corresponding power available to the ASIC input MOSFET branch is 2.8 mW. However the additional power required for voltage regulation, for the ASIC's common circuitry, and for biasing of the pixel spiral must be taken into account. Accordingly, in this version of the ASIC we limited the MOSFET power to about 0.5 mW, and dedicated more power to signal processing, thereby guaranteeing an overall high performance. In a next version, our choices might be revised. We note that for a standard pixel, which has an optimum area of about 650 μm^2, the corresponding optimum peaking time would exceed 30 μs, which is a factor of two higher than the value required by (1).

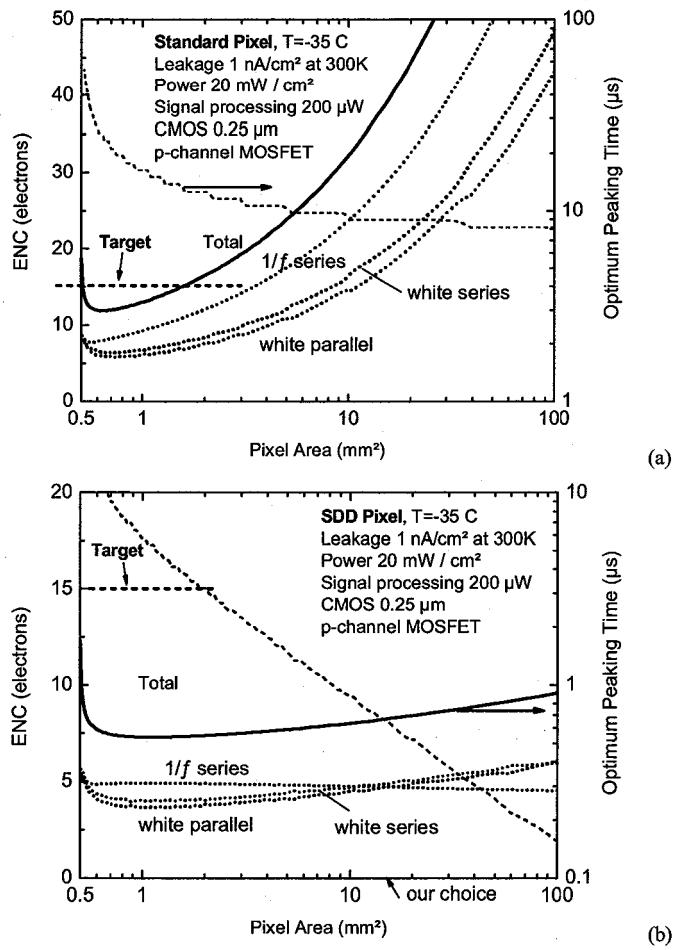


Fig. 3. Achievable ENC as function of the pixel area for the standard pixels (a) and SDD pixels (b).

III. Detector's Architecture

The sensor is composed of hexagonal SDD pixels, each 16 mm^2 in area (see Fig. 4). Each pixel behaves like an independent, small n-type drift detector with a central collecting anode. The drift field, parallel to the sensor's surface, is generated using a spiral geometry similar to that proposed in [22] and [23]; details on the sensor are given in [24]. The entrance side typically is biased at -80 V, the outer ring, common to all pixels, is biased at V_{OR} = -120 V, while the inner ring is biased at V_{IR} = 0V. The virtual ground of the front-end electronics, around 2 V, provides the final gradient for collecting the charge.

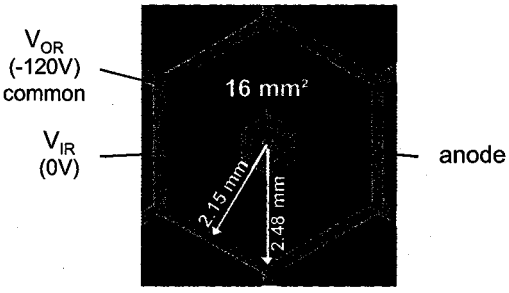
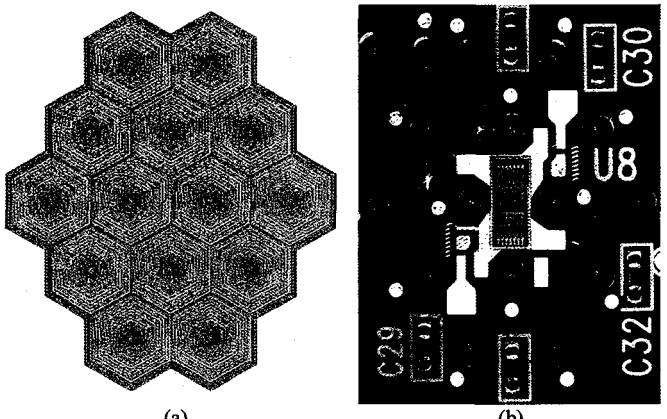


Fig. 4. Picture of the SDD pixel with an area 16 mm^2.

Fig. 5(a) shows the layout of a unit of 14 SDD pixels, having a total area of 224 mm^2. The anode of each SDD pixel is located at the center of the pixel and has a diameter around 200

μm (Fig. 4). The pixelated side of the unit is attached to one side of an interposer with a ≈ 2 mm hole in correspondence with each anode. There is a 14-channel ASIC on the other side of the interposer. Each anode is wire-bonded through the holes to one input of the 14 channels of the ASIC, as shown in Fig 5(b). Through the same holes the inner ring of the pixel is wire-bonded to the line that provides V_{IR} (depicted by the small dot near each hole in Fig. 5(b). One additional hole, in the upper left, provides the wire bond for V_{OR}. It can be easily verified that the resulting 14-element SDD-ASIC unit can be tiled to cover an arbitrarily large sensitive area. Since the ASIC dissipates about 25 mW, this represents 25 mW / 224 mm^2 ≈ 11 mW/cm^2, a value well within the requirement for the application.



(a) (b)

Fig. 5. Layout of the unit of 14 SDD pixels (a), with total area 224 mm^2, and picture of the interposer (b) with the SDD unit attached on the back side, with the ASIC, measuring 2 × 4.6 mm^2, attached on the front side. The 14 inputs of the ASIC are wire-bonded to the pixel anodes through 2 mm holes.

The electrons generated by the ionizing event are collected by the anode and read out by the ASIC that performs low-noise charge amplification, filtering, discrimination, peak detection with analog memory, and sparse readout. In the next Section, we describe the architecture of the ASIC.

IV. Architecture of the ASIC

Fig. 6 is a block diagram illustrating the architecture of the ASIC. The ASIC implements 14 front-end channels, multiplexers, common bias circuitry, registers, DACs, and control and readout logic.

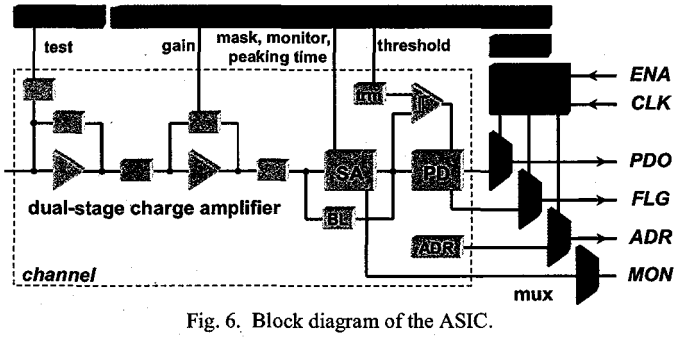


Fig. 6. Block diagram of the ASIC.

The charge amplifier is a dual-stage one with compensated adaptive continuous reset, similar to that described in [25] and [26], providing a total charge-gain adjustable to either 1024 or one third of that value. The first stage provides a charge gain of 32, and the second one a gain of 32 or 32/3, depending on the setting of a register. As shown in Fig. 7, an innovative aspect of this realization is the use of the MOSFETs M_{C1} and M_{C2} in the first charge gain stage, in place of capacitors. It can be easily verified that the non-linearity from M_{C1}, which has a capacitance of about 20 fF, is canceled by the compensation effect from the scaled replica M_{C2}.

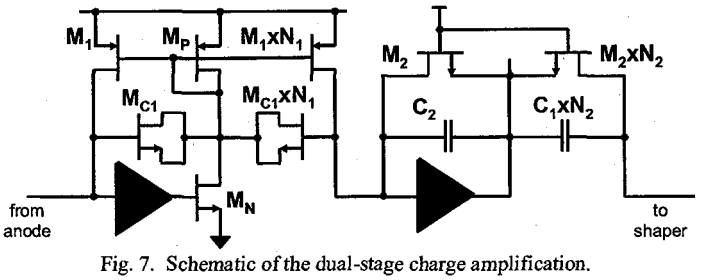


Fig. 7. Schematic of the dual-stage charge amplification.

The amplifier input MOSFET operates with a drain current of 200 μA and it is optimized for an input capacitance of 200 fF [21]. The dual-stage charge amplifier is followed by a 5th order shaper [27] with gain 3.3 mV/fC, a peaking time adjustable to 0.5-, 1-, 2-, and 4-μs, and an output baseline stabilized with a band-gap-referenced BLH circuit [28]. The overall channel gain can be adjusted to either 3.3 or 1.1 V/fC, thus covering an energy range up to 12 keV and 36 keV, respectively.

A low-hysteresis comparator with multiple-firing suppression [29] discriminates events, with a threshold controlled by a 10-bit DAC common to all channels, and a 3-bit DAC in each channel for equalization. The above-threshold events are processed by a multi-phase peak detector with an analog memory [29,30]. A flag (FLG), released after a first peak is found, indicates that one (or more) successful acquisition is ready to be read out. At each clock (CK) the peak amplitude (PDO) and the address (ADR) of all the events above threshold are made sequentially available at the dedicated outputs, thus providing sparsification. The readout process uses of both CMOS logic levels and Low Voltage Differential Signaling (LVDS). Additional functions include channel mask, channel test capacitor, on-chip test pulse generator with its amplitude controlled by a 10-bit DAC, monitor of channel shaper outputs and DAC voltages, and an optional function that disables the acquisition either when the first pulse crosses threshold, or at the first pulse peak.

Each channel also implements a pixel leakage current measurement circuit. The leakage current, multiplied by the gain of the charge amplifier, is absorbed by the BLH to maintain the output baseline at a constant voltage. A current source, controlled by the BLH and proportional to the leakage current, is converted into a voltage and it is made available by multiplexing through the analog monitor. The gain of this leakage current measurement circuit is about 1 mV/pA.

V. Preliminary Experimental Results

Our characterization of the ASIC brought into evidence a major issue with the ASIC layout. We found a parasitic capacitance of about 4 fF in parallel to the feedback MOSFET M_{C1} shown in Fig. 7. It resulted in a gain about 20 % lower than the design value, a mismatch in the pole-zero cancellation, and a noise somewhat larger than expected. The issue will be addressed in a revision; here we report the experimental results from the current version, although limited by this problem.

Fig. 8 shows the simulated- (lines) and measured- (symbols) ENC as function of the peaking time. The blue triangles and red circles represent measurements taken with the rms voltmeter connected to the analog monitor of the channel. The black diamonds signify measurements from a test pulse set at 0.3 fC (6.75 keV). All measurements were done at -35 C.

The blue triangles correspond to the case where the sensor was not connected to the input and with the internal 1.6 pA input current generator enabled. The blue line is the corresponding simulation; the difference between them is mainly due to the lower gain, with consequent increase of the contribution from the shaper.

The red circles correspond to the case with the sensor connected to the input and biased. The internal 1.6 pA input current generator is disabled. A leakage current of about 2.6 pA was extracted, and directly confirmed by measurements using the leakage current measurement circuit. The red line is the corresponding simulation, shown in Fig. 8 with the dominant noise contributions, viz., charge amplifier, leakage current (this includes the reset current), and shaper. In correspondence with the input capacitive load only the contribution from the charge amplifier increases, while the shaper's contribution remains the same (assuming a negligible drop in the gain with the input capacitive load).

The black diamonds are measurements acquired using the complete signal processing chain, i.e., encompassing the discriminator, peak detector, and multiplexing as described in the previous Section. The additional noise contribution is mainly related to the increase in current through the reset MOSFET during the discharge of the feedback capacitor after an event; it depends on the injected charge Q_{IN} (i.e., the energy of the event) [25]. In this case, the increase is of the order of 5.5 e^- rms at 0.3 fC (6.75 keV) although it is expected to be negligible at the few hundred eV spectral lines.

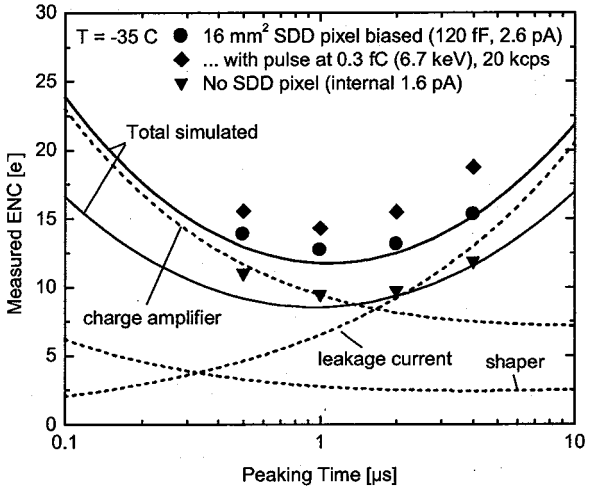


Fig. 8. Simulated and measured ENC versus peaking time without the sensor and with sensor connected and biased. The measurement with the test pulse peak at 6 keV is included. The dominant contributions to the ENC also are shown.

In Fig. 9 illustrates the ENC versus injected charge Q_{IN} (energy equivalent in Si), measured using the test pulse at 0.5 µs peaking time. The increase appears negligible when compared with the statistical fluctuations in the charge generated by the ionizing events, also depicted in Fig. 9. It can be seen that, due to the discussed ≈ 20 % deficit in gain, a charge corresponding to 16 keV could be injected, despite the design limit, at this gain setting, being just above 12 keV. An integral linearity error below +/- 0.4% was measured over the entire signal range of 2V.

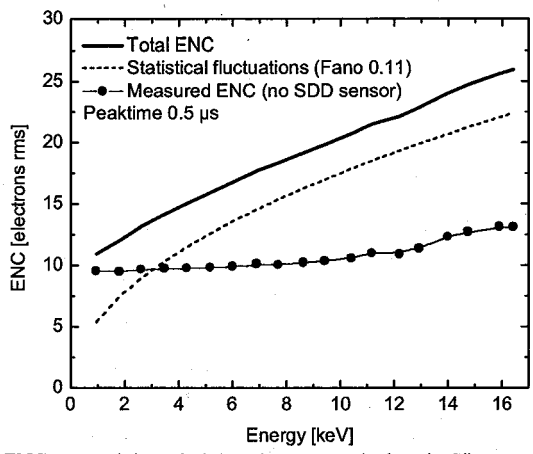


Fig. 9. ENC versus injected charge (energy equivalent in Si) measured using the test pulse. The simulated contribution due to statistical fluctuations (Fano limited), and the corresponding total ENC are included.

Fig. 10 shows the spectrum from an uncollimated ^{55}Fe source, measured at – 35 C, using the whole system with a peaking time of 1 µs, and a rate of 20 kcps. A resolution of 172 eV at 69.5 keV is observed, corresponding to 20.5 e^-. The contribution from the electronics is about 14.3 e^-, while Fano (0.11) contributes with 13.4 e^-. The residual 6.0 e^-, related to the sensor, still is being investigated.

Fig. 10 also illustrates a peak to background ratio of about 300 that was limited, in large amount, by charge sharing between the SDD pixels.

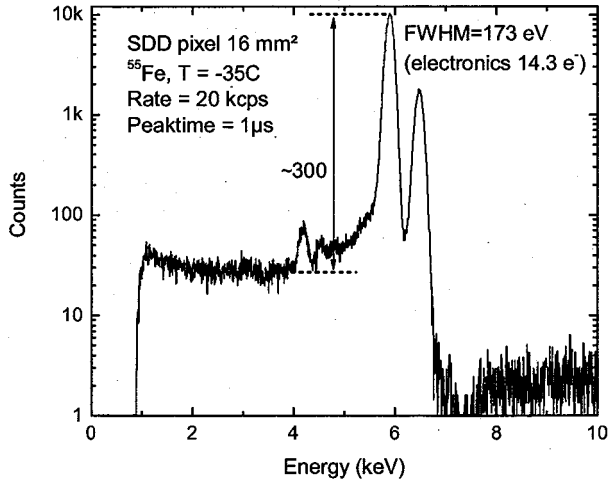


Fig. 10. Spectrum at -35 C, from a ^{55}Fe source measured with a peaking time of 1 µs, and a rate of 20 kcps.

Fig. 11(a) shows the spectra of ^{55}Fe at different rates ranging from 20 kcps up to 400 kcps, measured with a peaking time of 0.5 µs. There is considerable degradation at 400 kcps. Fig. 11(b) shows the corresponding FWHM for 0.5- and 1-µs peaking time. These measurements are affected by the poor pole-zero cancellation and are expected to improve in a revision.

We note that, given the pixel area of 16 mm^2, the requirement of 1 Mcps/cm^2 translates into about 150 kcps/pixel. At this rate, a resolution on the order of 170 keV at 6 keV appears achievable in a revision.

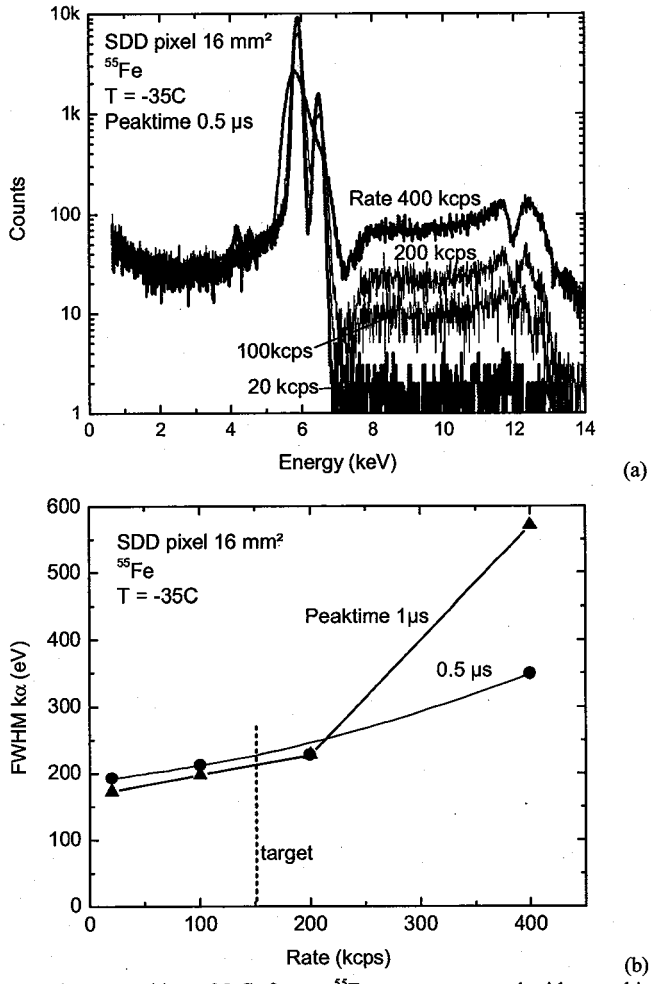


Fig. 11. Spectrum (a) at -35 C, from a ^{55}Fe source measured with a peaking time 0.5 µs, at rates from of 20- to 400-kcps; FWHM (b), at the k_α spectral line, with peaking times of 0.5- and 1-µs.

VI. Conclusions and Future Work

We developed and characterized the first prototype of a high resolution x-ray spectrometer, based on SDD pixels with direct readout through a low-noise ASIC, has been developed and characterized. Promising resolution was obtained. The ASIC requires a revision to eliminate some parasitic effects affecting the gain and pole-zero cancellation. With the current system, cooled at -35 C, resolutions of 173 eV and 200 eV at 59.5 keV can be achieved at pixel rates of 20 kcps and 150 kcps respectively.

Acknowledgments

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